



TITLE OF THE INVENTION

POWER AMPLIFIER AND RADIO COMMUNICATION DEVICE USING
THE AMPLIFIER

CROSS-REFERENCE TO RELATED APPLICATIONS

5 This application is based upon and claims the
benefit of priority from prior Japanese Patent
Application No. 2003-147917, filed May 26, 2003, the
entire contents of which are incorporated herein by
reference.

10 BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a power amplifier mainly for a high-frequency band, and more particularly to a power amplifier that selectively amplifies a plurality of input signals of different frequencies.

2. Description of the Related Art

There exist radio communication systems for providing services of mobile communication of a plurality of frequency bands. In such systems, radio communication devices, such as mobile terminals, are generally provided with the same number of transmission signal power amplifiers as that of frequency bands used.

For instance, in the personal digital cellular (PDC) system that uses two frequency bands, two power amplifiers for the 800-MHz band and 1900-MHz band are provided in a single mobile terminal. Even a mobile

terminal compatible with different systems, such as an 800-MHz-band PDC and 1900-MHz-band personal handy-phone system (PHS), is provided with power amplifiers dedicated to respective frequency bands.

5 In a radio communication device, such as a mobile terminal using a plurality of frequency bands, it is difficult to satisfy a demand for size reduction if power amplifiers dedicated to the respective frequency bands.

10 On the other hand, broadband amplifiers for use in measuring devices can amplify signals of different frequency bands. This type of amplifier, however, consumes much power, therefore is not suitable for mobile terminals that use a battery as a power supply.
15 For this reason, they are not used in mobile terminals.

BRIEF SUMMARY OF THE INVENTION

It is an object of the invention to provide a power amplifier for selectively amplifying signals of different frequency bands, which can be made compact,
20 and a radio communication device using the power amplifier.

According to an aspect of the invention, there is provided a power amplifier comprising: a first amplifier element configured to amplify a first input
25 signal of a first frequency, the first amplifier element including a first input terminal which receives the first input signal, and a first output terminal

which outputs a first output signal obtained by
amplifying the first input signal; a second amplifier
element configured to amplify an input signal of a
second frequency, the second amplifier element
5 including a second input terminal which receives the
input signal of the second frequency, and a second
output terminal which outputs a signal obtained by
amplifying the input signal of the second frequency; a
power supply input terminal connected to a direct-
10 current power supply; a common power supply path
including an end connected to the power supply input
terminal, and another end; a first individual power
supply path including an end connected to the another
end of the common power supply path, and another end
15 connected to the first output terminal, the first
individual power supply path having a first impedance;
and a second individual power supply path including an
end connected to the another end of the common power
supply path, and another end connected to the second
20 output terminal, the second individual power supply
path having a second impedance.

According to another aspect of the invention,
there is provided a power amplifier similar to the
above but further comprising: a first output matching
25 circuit connected to the first output terminal of the
first amplifier element; and a second output matching
circuit connected to the second output terminal of the

second amplifier element.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

FIG. 1A is a block diagram of a power amplifier according to a first embodiment of the invention;

5 FIG. 1B shows a FET used for each amplifier element in FIG. 1A;

FIG. 1C shows a bipolar transistor used for each amplifier element in FIG. 1A;

10 FIG. 2 is a diagram useful in explaining the impedance relationship between components in the first embodiment, assumed when an f1 amplifier element is operating;

15 FIG. 3 is a diagram useful in explaining the impedance relationship between components in the first embodiment, assumed when an f2 amplifier element is operating;

FIG. 4 illustrate the configuration of a power amplifier according to a second embodiment of the invention;

20 FIG. 5 is a diagram useful in explaining the impedance relationship between components in the second embodiment, assumed when an f3 amplifier element is operating;

25 FIG. 6 shows a first structure example of a power supply circuit incorporated in the first embodiment;

FIG. 7 shows a second structure example of the power supply circuit incorporated in the first

embodiment;

FIG. 8 shows a third structure example of the power supply circuit incorporated in the first embodiment;

5 FIG. 9 shows a fourth structure example of the power supply circuit incorporated in the first embodiment;

FIG. 10 shows a fifth structure example of the power supply circuit incorporated in the first
10 embodiment;

FIGS. 11A and 11B are schematic diagrams illustrating front and back specific structure examples of the power amplifier of the first embodiment;

FIGS. 12A ,12B and 12C are schematic diagrams illustrating plural side specific structure examples of
15 a power amplifier according to a third embodiment;

FIG. 13 is a block diagram of a multi-stage power amplifier according to a fourth embodiment; and

FIG. 14 is a block diagram of a radio
20 communication device according to a fifth embodiment.

DETAILED DESCRIPTION OF THE INVENTION

(First Embodiment)

FIG. 1A shows the configuration of a power amplifier according to a first embodiment of the
25 invention. The first embodiment will be described using, as an example, a power amplifier operable at two frequencies f_1 and f_2 .

The power amplifier has input terminals 11 and 12 for receiving input signals V_{i1} and V_{i2} of frequencies f_1 and f_2 . The input signal V_{i1} is input to the input terminal of an f_1 amplifier element 17 via an input matching circuit 14. The input signal V_{i2} is input to the input terminal of an f_2 amplifier element 18 via an input matching circuit 15. The signal amplified by the amplifier element 17 is output as an output signal V_{o1} from an output matching circuit 21. Similarly, the signal amplified by the amplifier element 18 is output as an output signal V_{o2} from an output matching circuit 22.

The amplifier elements 17 and 18 are formed of, for example, the FET as shown in FIG. 1B, or the bipolar transistor as shown in FIG. 1C. Further, each of the amplifier elements 17 and 18 is not always formed of a single transistor, but may be formed of, for example, two transistors connected in series. In FIG. 1A, reference numerals 1, 2 and 3 denote the control electrode and first and second main electrodes of the amplifier element 17. If the element 17 is formed of a FET, its gate electrode G, drain electrode D and source electrode S correspond to the control electrode and first and second main electrodes, respectively. Further, if the element 17 is formed of a bipolar transistor, its base electrode B, collector electrode C and emitter electrode E correspond

the control electrode and first and second main electrodes, respectively.

The signals output from the input matching circuits 14 and 15 are input to the respective control electrodes 1 of the amplifier elements 17 and 18. The signals amplified are output from the respective first main electrodes 2 of the amplifier elements 17 and 18. The second main electrodes 3 of the amplifier elements 17 and 18 are connected to a constant potential point (not shown), for example, grounded.

The supply of power, i.e., a DC voltage, to the amplifier elements 17 and 18 is performed by a power supply circuit described below. Firstly, one end of a common power supply path 31 is connected to a power supply input terminal 30 that is connected to a DC power supply Vcc. The common power supply path 31 is connected to both the amplifier elements 17 and 18. The other end of the common power supply path 31 is connected to one end of each of individual power supply paths 32 and 33 dedicated to the amplifier elements 17 and 18, respectively. The other ends of the lines 32 and 33 are connected to the respective first main electrodes of the amplifier elements 17 and 18. As described later, the individual power supply paths 32 and 33 have different impedances.

The operation of the power amplifier of the first embodiment will be described.

The f_1 and f_2 amplifier elements 17 and 18 operate at different frequencies f_1 and f_2 , as described above. However, they are controlled such that they operate exclusively. In other words, when one of the elements
5 17 and 18 is operating, the other is kept inoperative.

The output matching circuit 21 matches impedances with a circuit (not shown) connected after it, when the f_1 amplifier element 17 is operating at the frequency f_1 . The circuit 21 has a conjugate impedance
10 Z_{P1ON}^* with respect to the output impedance Z_{P1ON} of the amplifier element 17 during operation. Similarly, the output matching circuit 22 matches impedances with a circuit (not shown) connected after it, when the f_2 amplifier element 19 is operating at the frequency f_2 .
15 The circuit 22 has a conjugate impedance Z_{P2ON}^* with respect to the output impedance Z_{P2ON} of the amplifier element 18 during operation.

The output matching circuits 21 and 22 do not necessarily have conjugate impedances with respect to
20 the output impedances of the amplifier elements 17 and 18 during operation. They may be adapted to different purposes. For instance, the impedances of the output matching circuits 21 and 22 may be set so that the output signals V_{o1} and V_{o2} have the maximum levels
25 and/or the minimum distortion values.

FIG. 2 shows the impedances of the components of FIG. 1A assumed when the input signal V_{i1} of

the frequency f_1 is input to the input terminal 11, and the f_1 amplifier element 17 is operating and the f_2 amplifier element 18 is not operating. The operating amplifier element 17 has the output impedance Z_{P1ON} .

5 The first main electrode (output terminal) of the amplifier element 17 is connected to the output matching circuit 21 having the conjugate impedance Z_{P1ON}^* with respect to Z_{P1ON} , and is also connected to the power supply circuit. The power supply circuit has
10 the common power supply path 31 and individual power supply paths 32 and 33, as described above. DC power is supplied to the f_1 amplifier element 17 from the input terminal 30 via the common power supply path 31 and individual power supply path 32.

15 On the other hand, the f_2 amplifier element 18, which is not operating, has an output impedance Z_4 . The impedance Z_5 of the output matching circuit 22 connected to the first main electrode (output terminal) of the amplifier element 18 is identical to the
20 conjugate impedance Z_{P2ON}^* with respect to the output impedance Z_{P2ON} of the amplifier element 18 during operation.

Assuming that the synthesis impedance when the power supply circuit is viewed from the first main
25 electrode of the operating f_1 amplifier element 17 is Z_a , Z_a is given by

$$Z_a = \frac{Z_1(Z_3 + \frac{Z_4 Z_5}{Z_4 + Z_5}) + Z_2}{Z_2(Z_1 + Z_3 + \frac{Z_4 Z_5}{Z_4 + Z_5})} \quad (1)$$

where Z_1 represents the impedance of the common power supply path 31, Z_2 and Z_3 represent the impedances of the individual power supply paths 32 and 33, and $Z_2 \neq Z_3$. The impedances Z_1 , Z_2 and Z_3 are expressed as a frequency function, $Z_n(f) = R_n(f) + X_n(f)$ ($n = 1, 2, 3$). $R_n(f)$ represents the resistance component, and $X_n(f)$ the reactance component. In equation (1) directed to the case where the input signal V_{i1} of the frequency f_1 is input to the input terminal 11, and the f_1 amplifier element 17 is operating, Z_1 , Z_2 and Z_3 are $Z_1(f_1)$, $Z_2(f_1)$ and $Z_3(f_1)$, respectively.

At this time, if the real part $\text{Re}\{Z_a\}$ of the synthesis impedance Z_a is set higher than the real part $\text{Re}\{Z_{P1ON}^*\}$ of the impedance Z_{P1ON}^* of the output matching circuit 21, as shown in the following formula (2), the output signal (high frequency power) of the amplifier element 17 is efficiently guided to the output side via the output matching circuit 21, and output as the output signal V_{o1} .

$$\text{Re}\{Z_a\} > \text{Re}\{Z_{P1ON}^*\} \quad (2)$$

The greater the difference between $\text{Re}\{Z_a\}$ and $\text{Re}\{Z_{P1ON}^*\}$, the higher the effect. If $\text{Re}\{Z_a\}$ is five times or more $\text{Re}\{Z_{P1ON}^*\}$, and more preferably if

the former is ten times or more the latter, the greater part of the high-frequency power of the output signal of the f1 amplifier element 17 can be output as the output signal Vol.

5 FIG. 3 shows the impedances of the components of FIG. 1A assumed when the input signal Vi2 of the frequency f2 is input to the input terminal 12, and the f2 amplifier element 18 is operating and the f1 amplifier element 17 is not operating. The operating
10 amplifier element 18 has the output impedance Z_{P2ON} . The first main electrode (output terminal) of the amplifier element 18 is connected to the output matching circuit 22 having the conjugate impedance Z_{P2ON}^* with respect to Z_{P2ON} , and is also connected to
15 the power supply circuit. In the power supply circuit, DC power is supplied to the f2 amplifier element 18 from the input terminal 30 via the common power supply path 31 and individual power supply path 33.

On the other hand, the f1 amplifier element 17,
20 which is not operating, has an output impedance Z_6 . The impedance Z_7 of the output matching circuit 21 connected to the first main electrode (output terminal) of the amplifier element 17 is identical to the conjugate impedance Z_{P1ON}^* with respect to the output
25 impedance Z_{P1ON} of the amplifier element 17 during operation.

Assuming that the synthesis impedance when the

power supply circuit is viewed from the first main electrode of the operating f2 amplifier element 18 is Zb, Zb is given by

$$Z_b = \frac{Z_1(Z_2 + \frac{Z_6 Z_7}{Z_6 + Z_7}) + Z_3}{Z_3(Z_1 + Z_2 + \frac{Z_6 Z_7}{Z_6 + Z_7})} \quad (3)$$

In equation (3) directed to the case where the input signal Vi2 of the frequency f2 is input to the input terminal 12, and the f2 amplifier element 18 is operating, Z1, Z2 and Z3 in the equation (3) are Z1(f2), Z2(f2) and Z3(f2), respectively.

At this time, if the real part Re{Zb} of the synthesis impedance Zb is set higher than the real part Re{Zp2ON*} of the impedance Zp2ON* of the output matching circuit 22, as shown in the following formula (4), the output signal (high frequency power) of the amplifier element 18 is efficiently guided to the output side via the output matching circuit 22, and output as the output signal Vo2.

$$\text{Re}\{Z_b\} > \text{Re}\{Z_{P2ON}^*\} \quad (4)$$

Also in this case, if Re{Zb} is five times or more Re{Zp2ON*}, and more preferably if the former is ten times or more the latter, the greater part of the high-frequency power of the output signal of the f2 amplifier element 18 can be output as the output signal Vo2.

From the above formulas (1) to (4), Z_1 , Z_2 and Z_3 are determined.

As described above, the power supply circuit for supplying power to the amplifier elements 17 and 18 comprises the common power supply path 31 commonly provided for the amplifier elements 17 and 18, and the individual power supply paths 32 and 33 provided for the amplifier elements 17 and 18, respectively, and having different impedances. By virtue of this structure, the power amplifier can be made compact.

The advantage of the above structure will now be described. Assume that the area of the common power supply path 31 is S_1 , and those of the individual power supply paths 32 and 33 are S_2 and S_3 , respectively. In a power amplifier having a single amplifier element operable at a single frequency, the power supply circuit needs an area of $(S_1 + S_2)$ or $(S_1 + S_3)$ (i.e., the sum of the area S_1 of the common power supply path and one of the areas S_2 and S_3 of the individual power supply paths). Accordingly, where two individual power supply circuits are provided for two amplifier elements, an area of $(2S_1 + S_2 + S_3)$ is needed.

On the other hand, the area of the power supply circuit employed in the embodiment is $(S_1 + S_2 + S_3)$, which is smaller by S_1 than the case where individual power supply circuits are provided for two amplifier elements. Since, in general, the power supply circuit

occupies a relatively large area in the power amplifier, reduction of the area of the power supply circuit significantly contributes to the reduction of the size of the power amplifier.

5 In the embodiment, the output matching circuits 21 and 22 are set to have conjugate impedances with respect to the output impedances of the amplifier elements 17 and 18 during operation, respectively. However, the impedances of the circuits 21 and 22 are
10 not limited to the conjugate ones, but may be varied in accordance with purposes.

(Second Embodiment)

 The power amplifier of the first embodiment is operable at two frequencies f_1 and f_2 . However, a
15 power amplifier that is operable at three or more frequencies can be realized. In this case, it is sufficient if the power amplifier comprises three or more amplifier elements, a single common power supply path, three or more individual power supply paths and
20 three or more output matching circuits. FIG. 4 shows a power amplifier according to a second embodiment, which is operable at three frequencies f_1 , f_2 and f_3 . In FIGS. 4 and 5, elements similar to those in FIG. 1A are denoted by corresponding reference numerals.

25 The second embodiment employs a f_3 amplifier element 19, as well as the f_1 and f_2 amplifier elements 17 and 18. DC power input to the power supply input

terminal is supplied to one end of the common power supply path 31. After that, the DC power is distributed to the f1 amplifier element 17 via the individual power supply path 32, to the f2 amplifier element 18 via the individual power supply path 33, and to the f3 amplifier element 19 via the individual power supply path 34. The individual power supply paths 32, 33 and 34 have different impedances, as will be described later.

FIG. 5 shows the impedances of the components of FIG. 4 assumed when an input signal V_{i3} of a frequency f_3 is input to an input terminal 13, and the f1 and f2 amplifier elements 17 and 18 are not operating and the f3 amplifier element 19 is operating. The operating amplifier element 19 has an output impedance Z_{p3ON} . The first main electrode (output terminal) of the amplifier element 19 is connected to an output matching circuit 23 having a conjugate impedance Z_{p3ON}^* with respect to Z_{p3ON} , and is also connected to the power supply circuit.

On the other hand, the f1 amplifier element 17, which is not operating, has an output impedance Z_6 . The impedance Z_7 of the output matching circuit 21 connected to the first main electrode (output terminal) of the amplifier element 17 is identical to the conjugate impedance Z_{p1ON}^* with respect to the output impedance Z_{p1ON} of the amplifier element 17 during

operation. Similarly, the f2 amplifier element 18, which is not operating, has an output impedance Z4. The impedance Z5 of the output matching circuit 22 connected to the first main electrode (output terminal) of the amplifier element 18 is identical to the conjugate impedance Z_{P2ON}^* with respect to the output impedance Z_{P2ON} of the amplifier element 18 during operation.

Assuming that the synthesis impedance when the power supply circuit is viewed from the first main electrode of the operating f3 amplifier element 19 is Z_c , Z_c is given by

$$Z_c = Z_8 + \frac{Z_1(Z_3 + \frac{Z_4 Z_5}{Z_4 + Z_5})(Z_2 + \frac{Z_6 Z_7}{Z_6 + Z_7})}{(Z_3 + \frac{Z_4 Z_5}{Z_4 + Z_5})(Z_2 + \frac{Z_6 Z_7}{Z_6 + Z_7}) + Z_1(Z_3 + \frac{Z_4 Z_5}{Z_4 + Z_5}) + Z_1(Z_2 + \frac{Z_6 Z_7}{Z_6 + Z_7})} \quad (5)$$

In equation (5) directed to the case where the input signal V_{i3} of the frequency f_3 is input to the input terminal 13, and the f3 amplifier element 19 is operating, Z_1 , Z_2 and Z_3 are $Z_1(f_3)$, $Z_2(f_3)$ and $Z_3(f_3)$, respectively.

Similarly, the synthesis impedance Z_a , obtained if the power supply circuit is viewed from the first main electrode of the f1 amplifier element 17 when the element 17 is operating and the elements 18 and 19 are not operating, is given by the following equation (6). The synthesis impedance Z_b , obtained if the power

supply circuit is viewed from the first main electrode of the f2 amplifier element 18 when the element 18 is operating and the elements 17 and 19 are not operating, is given by the following equation (7).

5

$$Z_a = Z_2 + \frac{Z_1(Z_3 + \frac{Z_4 Z_5}{Z_4 + Z_5})(Z_8 + \frac{Z_9 Z_{10}}{Z_9 + Z_{10}})}{(Z_3 + \frac{Z_4 Z_5}{Z_4 + Z_5})(Z_8 + \frac{Z_9 Z_{10}}{Z_9 + Z_{10}}) + Z_1(Z_3 + \frac{Z_4 Z_5}{Z_4 + Z_5}) + Z_1(Z_8 + \frac{Z_9 Z_{10}}{Z_9 + Z_{10}})} \quad (6)$$

10

$$Z_b = Z_3 + \frac{Z_1(Z_2 + \frac{Z_6 Z_7}{Z_6 + Z_7})(Z_8 + \frac{Z_9 Z_{10}}{Z_9 + Z_{10}})}{(Z_2 + \frac{Z_6 Z_7}{Z_6 + Z_7})(Z_8 + \frac{Z_9 Z_{10}}{Z_9 + Z_{10}}) + Z_1(Z_2 + \frac{Z_6 Z_7}{Z_6 + Z_7}) + Z_1(Z_8 + \frac{Z_9 Z_{10}}{Z_9 + Z_{10}})} \quad (7)$$

In equation (6) directed to the case where the input signal Vi1 of the frequency f1 is input to the input terminal 11, and the f1 amplifier element 17 is operating, Z1, Z2 and Z3 are Z1(f1), Z2(f1) and Z3(f1), respectively. Similarly, in equation (7) directed to the case where the input signal Vi2 of the frequency f2 is input to the input terminal 12, and the f2 amplifier element 18 is operating, Z1, Z2 and Z3 are Z1(f2), Z2(f2) and Z3(f2), respectively.

20

In those cases, if the real parts Re{Za}, Re{Zb} and Re{Zc} of the synthesis impedances Za, Zb and Zc are set higher than the real parts Re{Zp1ON*}, Re{Zp2ON*} and Re{Zp3ON*} of the impedances Zp1ON*, Zp2ON* and Zp3ON* of the output matching circuits 21, 22 and 23, respectively, as shown in the following

25

formulas (8), (9) and (10), the output signals (high frequency power) of the amplifier elements 17, 18 and 19 are efficiently guided to the output side via the output matching circuits 21, 22 and 23, and output as the output signals Vo1, Vo2 and Vo3, respectively.

$$\operatorname{Re}\{Z_a\} > \operatorname{Re}\{Z_{P1ON}^*\} \quad (8)$$

$$\operatorname{Re}\{Z_b\} > \operatorname{Re}\{Z_{P2ON}^*\} \quad (9)$$

$$\operatorname{Re}\{Z_c\} > \operatorname{Re}\{Z_{P3ON}^*\} \quad (10)$$

From the formulas (1) to (10), Z1, Z2 and Z3 are determined. Even in the case of a power amplifier including four or more amplifier elements, the impedances of the common power supply path and individual power supply paths can be determined by executing the same procedure as the above.

Moreover, as in the first embodiment, if the real parts $\operatorname{Re}\{Z_a\}$, $\operatorname{Re}\{Z_b\}$ and $\operatorname{Re}\{Z_c\}$ of the synthesis impedances Z_a , Z_b and Z_c are five times or more $\operatorname{Re}\{Z_{P1ON}^*\}$, $\operatorname{Re}\{Z_{P3ON}^*\}$ and $\operatorname{Re}\{Z_{P2ON}^*\}$, respectively, and more preferably if the formers are ten times or more the latters, the greater part of the high-frequency power of the output signals of the f1, f2 and f3 amplifier elements 17, 18 and 19 can be output as the output signals Vo1, Vo2 and Vo3.

A description will be given of more specific power amplifier examples according to the first and second embodiments.

FIG. 6 shows a first example of the power amplifier of the first embodiment that is operable at the frequencies f_1 and f_2 . In this example, the power supply circuit is formed of a plurality of spiral inductors. A spiral inductor 41 corresponds to the common power supply path 31, and spiral inductors 42 and 43 correspond to the individual power supply paths 32 and 33, respectively. The impedances of the spiral inductors 41, 42 and 43 are given by

$$Z_1 = R_1 + j\omega X_1 \quad (11)$$

$$Z_2 = R_2 + j\omega X_2 \quad (12)$$

$$Z_3 = R_3 + j\omega X_3 \quad (13)$$

where R_1 , R_2 and R_3 represent the resistance components, and X_1 , X_2 and X_3 the reactance components. R_1 , R_2 , R_3 , X_1 , X_2 and X_3 can be determined by combining the equations (11), (12) and (13) with the formulas (1), (2), (3) and (4), and setting an appropriate frequency.

FIG. 7 shows a second example of the power amplifier of the first embodiment. In this example, the power supply circuit is formed of meander lines and capacitors. A meander line 51 corresponds to the common power supply path 31, and meander lines 52 and 53 correspond to the individual power supply paths 32 and 33, respectively. Capacitors 54, 55 and 56 are provided between the input terminals of the meander

lines 51, 52 and 53 and the earth, respectively.

FIG. 8 shows a third example of the power amplifier of the first embodiment. In this example, the power supply circuit is formed of transmission
5 lines and bonding wires. A straight transmission line 61A, T-shaped transmission line 61B and bonding wire 64 connecting them provide a common power supply path corresponding to the common power supply path 31 in FIG. 1A. The T-shaped transmission line 61B,
10 transmission line 62 and bonding wire 65 connecting them provide an individual power supply path corresponding to the individual power supply path 32 in FIG. 1A. Similarly, the T-shaped transmission line 61B, transmission line 63 and bonding wire 66 connecting them
15 provide an individual power supply path corresponding to the individual power supply path 33 in FIG. 1A. Desired impedances can be obtained by changing the lengths and/or thicknesses of the bonding wires 64, 65 and 66.

20 FIG. 9 shows a fourth example of the power amplifier of the first embodiment. In this example, the power supply circuit is formed of chip components that include capacitors and inductors. A capacitor 71 and inductor 72 provide a common power supply path
25 corresponding to the common power supply path 31 in FIG. 1A. A capacitor 73 and inductor 74 provide an individual power supply path corresponding to the

individual power supply path 32 in FIG. 1A, while a capacitor 75 and inductor 76 provide an individual power supply path corresponding to the individual power supply path 33 in FIG. 1A.

5 FIG. 10 shows a fifth example of the power amplifier of the first embodiment. In this example, the power supply circuit is formed of inductors or median lines using via holes. Specifically, wiring layers 81 and 82 on the upper and lower surfaces of a
10 plate 80 called a module plate, respectively. Each of the wiring layers 81 and 82 has a transmission line 83 of a predetermined pattern. The upper and lower surfaces of the substrate 80 are connected to each other by via holes 84, thereby forming inductors or
15 median lines.

 Also in the second to fifth examples, R_1 , R_2 , R_3 , X_1 , X_2 and X_3 can be determined by combining the equations (11), (12) and (13) with the formulas (1), (2), (3) and (4), and setting an appropriate frequency.

20 FIGS. 11A and 11B shows front and back structures of a sixth example of the power amplifier of the first embodiment, respectively. In this example, the amplifier elements and power supply circuit are provided on different layers of a multilayer substrate.
25 Specifically, the f_1 and f_2 amplifier elements 17 and 18 and individual power supply paths 32 and 33 are provided on the upper surface of a multilayer substrate

90, while the common power supply path 31 is provided on the lower surface of the substrate 90.

(Third Embodiment)

FIGS. 12A ,12B and 12C show, respectively, plural
5 structures of a power amplifier according to a third
embodiment that is operable at the four frequencies f1,
f2, f3 and f4. This power amplifier employs the
structure shown in FIG. 11A and 11B. Specifically, f1
and f2 amplifier elements 17 and 18 and individual
10 power supply paths 22 and 23 are provided on the upper
surface 91 of a multilayer substrate. A common power
supply path 21 is provided on the intermediate layer 92
of the substrate. Further, f3 and f4 amplifier
elements 19 and 20 and individual power supply paths 24
15 and 25 are provided on the lower surface 93 of the
substrate.

(Fourth Embodiment)

FIG. 13 shows a power amplifier according to a
fourth embodiment of the invention. The power
20 amplifiers of the first and second embodiments have a
single-stage structure, while the power amplifier of
the fourth embodiment has a dual-stage structure.

In the fourth embodiment, input signals Vi1 and
Vi2 of frequencies f1 and f2, supplied to input
25 terminals 11 and 12, are input to the first-stage f1
and f2 amplifier elements 17A and 18A via input
matching circuits 14 and 15, respectively. The outputs

of the first-stage f1 and f2 amplifier elements 17A and 18A are input to the second-stage f1 and f2 amplifier elements 17B and 18B via intermediate matching circuits 24 and 25, respectively. The outputs of the second-
5 stage f1 and f2 amplifier elements 17B and 18B are extracted as output signals Vo1 and Vo2 via output matching circuits 21 and 22, respectively.

DC power is supplied to the first-stage f1 and f2 amplifier elements 17A and 18A via a first power supply
10 circuit that has a common power supply path 31A and individual power supply paths 32A and 33A. Similarly, DC power is supplied to the second-stage f1 and f2 amplifier elements 17B and 18B via a second power supply circuit that has a common power supply path 31B
15 and individual power supply paths 32B and 33B. The fourth embodiment can be modified into a power amplifier including a three-stage or more structure.
(Fifth Embodiment)

A description will be given of a radio
20 communication device according to a fifth embodiment of the invention, in which the power amplifier of the first embodiment is incorporated in the transmission system of the device. FIG. 14 shows the configuration of a radio communication device operable at two
25 frequency bands.

Firstly, the receiving system of the device will be described. An RF reception signal received by

an antenna 100 is guided to the receiving system via a duplexer 101, and distributed into two receiving routes by a switch 102 in accordance with its frequency. If the RF signal is distributed into a first receiving route, it is guided to a mixer 107 via a band-pass filter (BPF) 103 and low noise amplifier (LNA) 105, and is subjected to frequency conversion based on a local signal from a local signal source 109, i.e., it is down-converted.

The output signal of the mixer 107 is simultaneously input to two mixers 112 and 113 via a band-pass filter 110. The mixers 112 and 113 provide an orthogonal demodulator, receive orthogonal local signals from a local signal source 114, and convert the signals, supplied from the band-pass filter 110, into orthogonal reception baseband signals, i.e., I and Q signals. The orthogonal reception baseband signals are input to a baseband processing unit 120, where they are reproduced as received data.

A second receiving route is similar to the first one, and comprises a band-pass filter 104, low noise amplifier 106, mixer 108, band-pass filter 108, mixers 115 and 116, and local signal source 117. The local signal source 117 generates local signals of a frequency different from that of the local signals generated by the local signal source 114.

The transmission system will now be described.

The baseband processing unit 120 performs digital signal processing on transmission data, thereby generating orthogonal transmission baseband signals, i.e., I and Q signals. The generated I/Q signals are
5 input to one of the transmission routes in accordance with their transmission frequency. If the I/Q signals are input to a first transmission route, they are multiplied, in mixers 121 and 122, by the respective orthogonal local signals from a local signal
10 source 123. The output signals of the mixers 121 and 122 are added by an adder 127. The mixers 121 and 122 and adder 127 form an orthogonal modulator.

The output signal of the adder 127 is guided to a mixer 129, where it is subjected to frequency
15 conversion based on a local signal from a local signal line 131, i.e., it is up-converted. The output signal of the mixer 129 is supplied to a band-pass filter 132, where an unnecessary component is eliminated therefrom. After that, the resultant signal is amplified by
20 a power amplifier 134. The output signal of the power amplifier 134 is guided to a switch 137 via a low-pass filter 135, and then to the antenna 100 via the duplexer 101. Thus, the signal is output as an electric wave from the antenna.

25 The other transmission route, i.e., a second route, is similar to the first one, and comprises mixers 124 and 125 and adder 128 providing

an orthogonal modulator, local signal source 126 for the orthogonal modulator, mixers 129 and 130 and local signal line 131 for up-conversion, band-pass filter 133, power amplifier 134 and low-pass filter 136.

5 The transmission frequency, i.e., the frequency of a transmission signal input to the power amplifier 134, differs from that of the first transmission route.

If the power amplifier of the first embodiment is used as the power amplifier 134, it can be commonly
10 used for two transmission routes. This being so, the whole area required for the power amplifier can be reduced compared to the case where respective power amplifiers are used for two transmission routes, which contributes to the reduction of the size and cost of
15 the radio communication device. Further, a radio communication device having three or more frequencies can be realized by modifying the configuration of
FIG. 14.

Additional advantages and modifications will
20 readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the
25 spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.